# Experiment Name:

# Implementation and Design of full adder circuit using ASIC design tools. Y=and Carry=AB+BC+CA

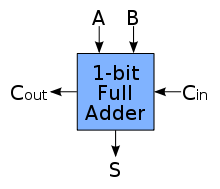
## *Objectives:*

1. To implement NAND and XOR gate
2. To simulate our design in three different ways:
   * Circuit design and Logic verification using DSCH.
   * Circuit design simulation and Logic verification using DSCH and µ-wind.
   * Layout design simulation using Micro wind.
3. To observe the deviation in results with default layout and our manual layout.

***Component:* DSCH software,µ-wind software**

## *Discription*:

***Full Adder:***



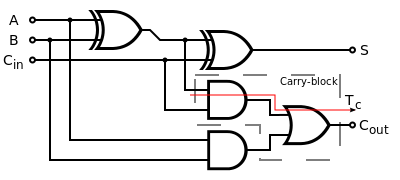


Fig: Block Diagram of Full Adder Fig: Logic Diagram for Full adder

***The NAND Gate:***

The truth-table and logic symbol of the AND,OR,XOR gate and with 3 inputs are shown below.

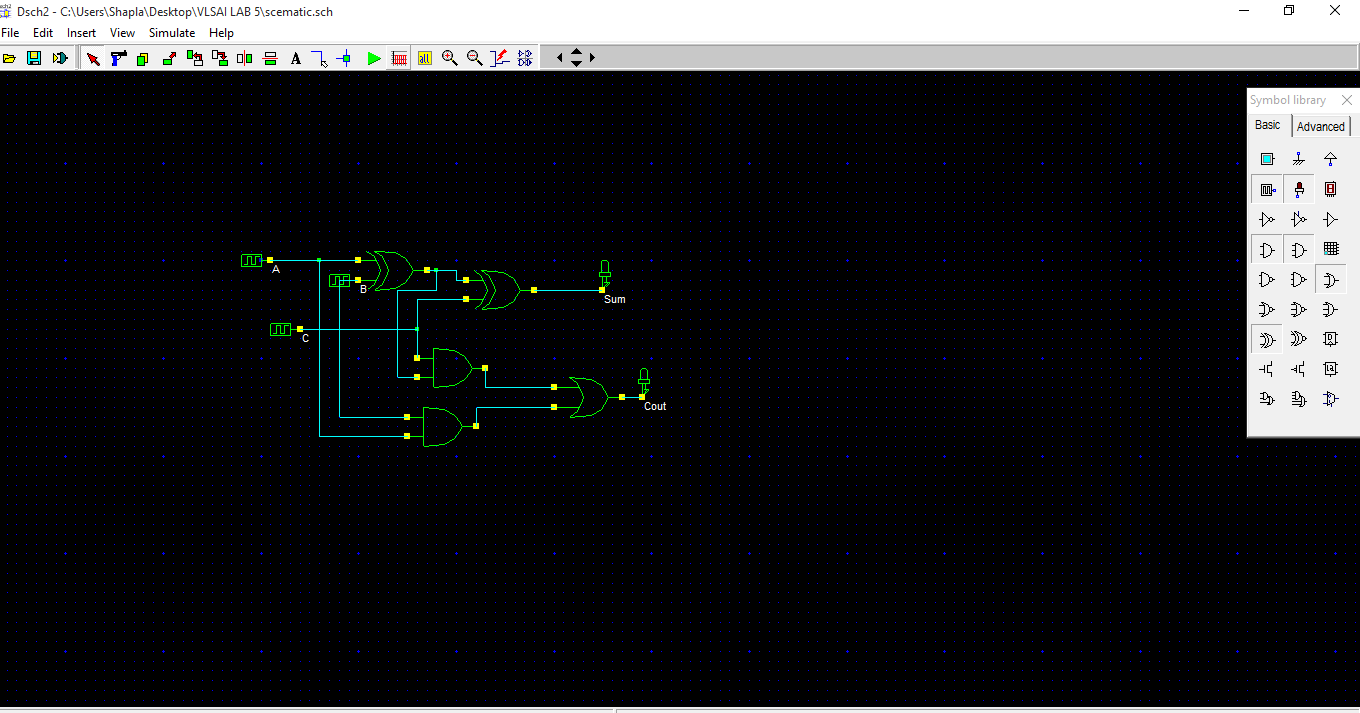
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# The truth table and symbol of Y=and Carry=AB+BC+CA

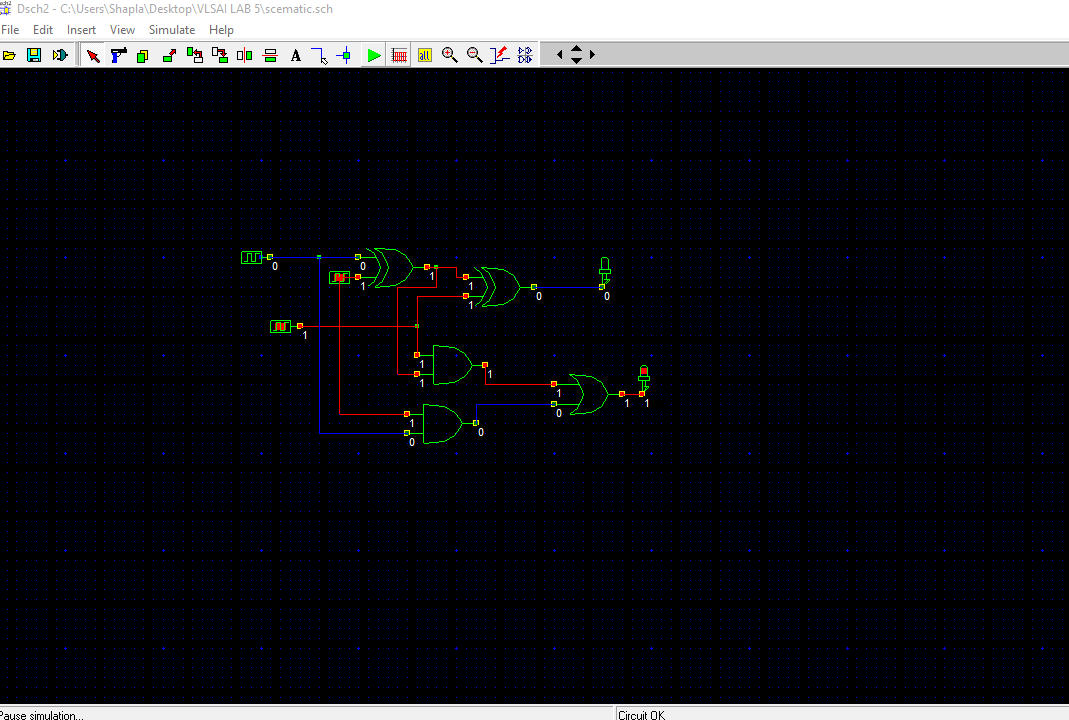
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| INPUT | | | **OUTPUT** | |
| A | B | C | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

***Working Principles:***

* Design the schematic diagram of the full adder circuit using DSCH2.



* Check the timing diagram to see if the designed circuit is correct and follows the truth table given above.



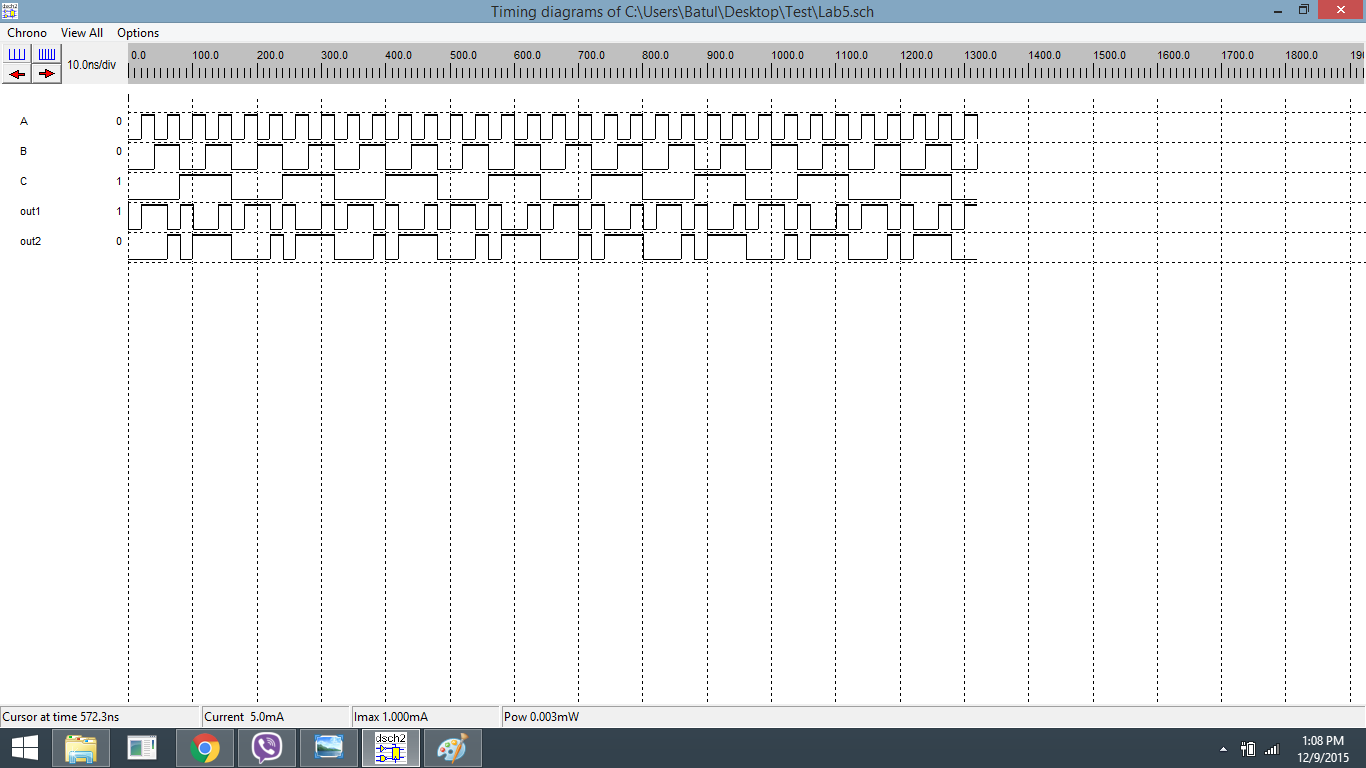


Figure: Timing diagram of the full adder circuit

* Make a Verilog file of the .sch file in DSCH2.

// DSCH 2.6h

// 08-Dec-15 3:41:12 PM

// C:\Users\Shapla\Desktop\scematic.sch

module scematic( A,C,B,Sum,Cout);

input A,C,B;

output Sum,Cout;

xor #(23) xor2(w3,A,B);

xor #(16) xor2(Sum,w3,C);

and #(16) and2(w6,w3,C);

and #(16) and2(w7,A,B);

or #(16) or2(Cout,w6,w7);

endmodule

// Simulation parameters in Verilog Format

always

#16000 A=~A;

#8000 C=~C;

#2000 B=~B;

// Simulation parameters

// A CLK 160.000 160.000

// C CLK 80.000 80.000

// B CLK 20.000 20.000

* In microwind, compile the Verilog file saved in DSCH2 and implement the layout of the circuit.

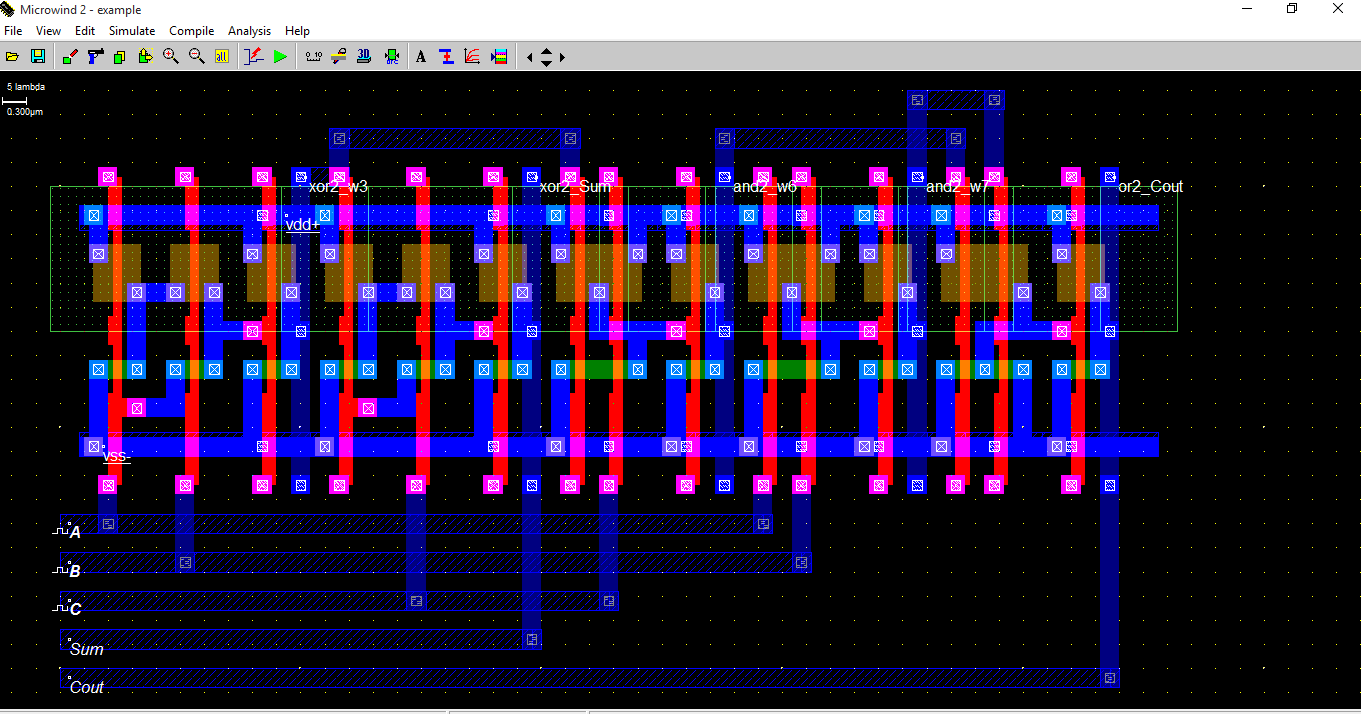


Figure : Implemented layout from the Verilog file.

* Check the simulated waveform to verify the truth table.

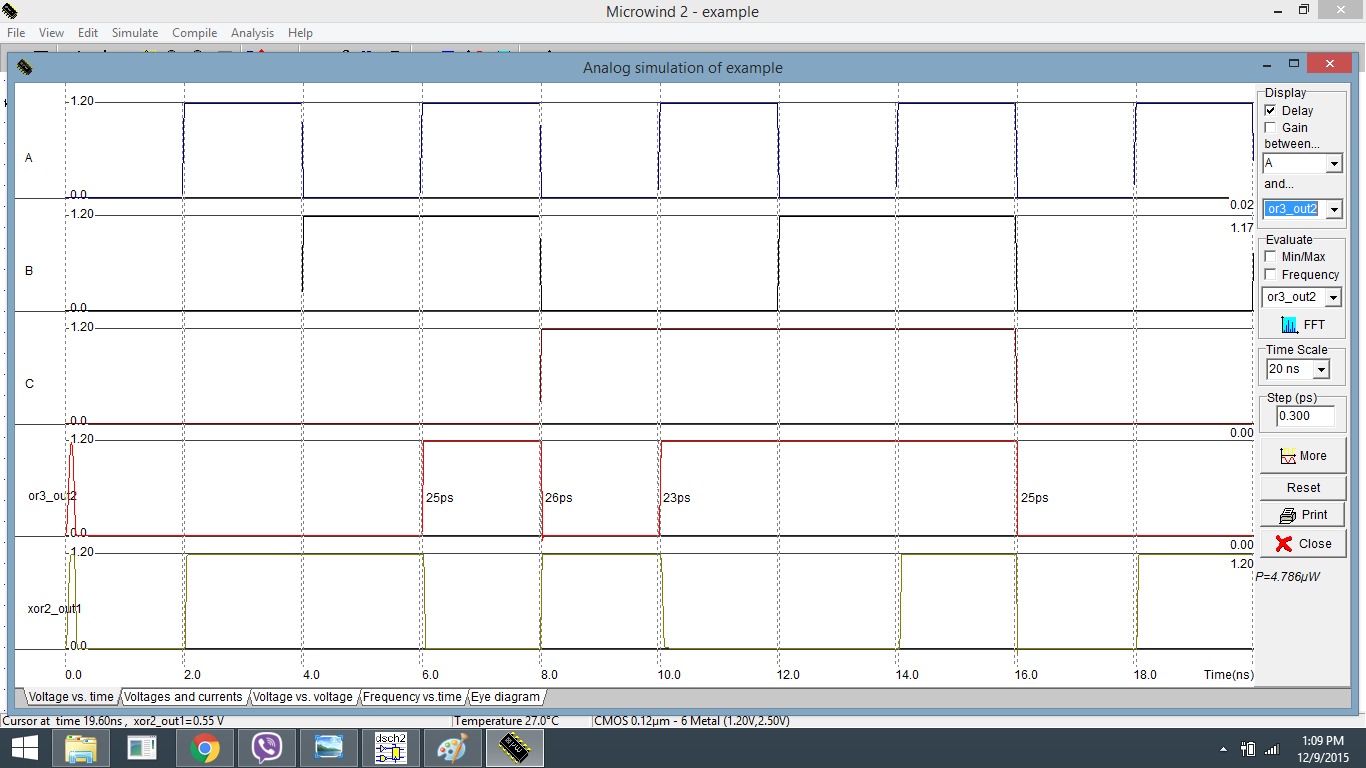


Figure-4: Simulated waveform using microwind of the full adder circuit

***Conclusion:***

The NAND gate is implemented using two XOR, three AND, one OR gate and the truth table is successfully verified. The required waveforms were obtained, observed and noted down using microwind2.

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